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AN OVERVIEW OF DIFFERENT POWER OPTIMIZATION DESIGNS FOR ADIABATIC SWITCHING

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ABSTRACT

Energy efficiency is the critical feature of modern electronic systems, due to desirability of portable devices, demand for reliability and performance, to extend battery life, need to reduce package cost, to reduce Green cost etc. Advancements in scaling with reduced threshold and supply voltages lead to increased leakages in MOS transistors. Many studies presented that leakage power consumption is up to 40% of total power consumption in nanometre technology. To overcome the power dissipation problem many researchers have proposed different ideas from the device level to the architectural level. However, there is no universal way to avoid trade-offs between power, delay and area. Thus, designers are required to choose appropriate techniques that satisfy application and product needs. In VLSI circuits, to control the power consumption supply voltage plays an important role. Supply voltage scaling without scaling of threshold voltage degrades the performance of the device. The reduction of threshold voltage and supply voltages proportionally retains the performance. The threshold voltage reduction leads to five times higher leakage current. The requirements for power optimization continue to increase significantly and the motivations to optimise power differ from application to application. Power consumption has become primary design issue and needs suitable power management in the design of digital circuits where switching and standby mode affects the performance of system. The design of a low power circuits mainly focuses on a problem occurred due to the performance, power dissipation and chip area.

Keywords: Power Optimization Designs, MOS Transistors, Threshold Voltage, Supply Voltages.